REMARKS

A. Introduction

In the Office Action mailed October 12, 2006, the Examiner rejected claims 26-29, 31-32, 35-39, 41-42, 45, 47-50, 52-53 and 56 under 35 U.S.C. § 112, first paragraph and rejected claims 1-17 and 26-45 under 35 U.S.C. §112, second paragraph. In addition, the Examiner rejected claims 18-25, 46 and 54-55 under 35 U.S.C. §102(e) over Wooten (U.S. Patent No. 5,832,299). The Examiner rejected claims 1-17, 33, 34, 43 and 44 under 35 U.S.C. §103(a) over a combination of Wooten and Russell (U.S. Patent No. 6,751,737). The Examiner also rejected claims 47-53 and 56 under 35 U.S.C. §103(a) over a combination of Wooten and common knowledge in the art. The Examiner rejected claims 26-32, 35-42 and 45 under 35 U.S.C. §103(a) over a combination of Wooten, Russell, and common knowledge in the art. Applicant herein amends claims 1, 5, 18-20, 22, 24-27, 29, 36-37, 39, 47-48, and 50-54 to more clearly identify the subject matter for which applicant seeks protection. Also, applicant has canceled claims 28, 35, 38, 45-46, 49, and 56. As a result, claims 1-27, 29-34, 36-37, 39-44, 47-48, and 50-55 are now pending. For reasons discussed in detail below, applicant submits that the pending claims are now in condition for allowance.

B. Rejections Under 35 U.S.C. § 112, first paragraph

The Examiner rejected claims 26-29, 31-32, 35-39, 41-42, 45, 47-50, 52-53, and 56 under 35 U.S.C. § 112, first paragraph. Specifically, the Examiner argues that the specification does not support "receiving a signal on a package pin of the processor, receiving a message via an APIC bus or front side bus, receiving the SMI from a Northbridge or Southbridge controller, or indicating a cause that triggered the SMI." (Office Action, Page 3). Applicant has canceled claims 28, 35, 38, 45, 49, and 56 and has amended the claims to recite receiving a signal on "an input line of the processor" (claims 26, 36, and 47), such as "an SMI input line" (claims 27, 37, and 48). Support for this amendment can be found, for example, on page 3 of applicant's specification, which

provides that "an SMI is generated when an SMI input line to the processor is set by the chipset." (Applicant's specification, Page 3). Because applicant's specification clearly teaches receiving a signal via an input line of the processor (claims 26, 36, and 47), such as an SMI input line (claims 27, 37, and 48), applicant respectfully requests that the Examiner reconsider and withdraw the rejection of claims 26-27, 36-37, and 47-48 under 35 U.S.C. § 112, first paragraph.

Also, because one having ordinary skill in the art at the time the application was filed would have known that the term "chipset" often refers to the two main motherboard chips: Northbridge and Southbridge (*See e.g.*, page 7 of Intel® Pentium® II Processor – Low Power Datasheet, Document Reference Number 273268-001, September 1999; attached herein), applicant's specification supports that a processor chipset, such as a northbridge controller (claims 31, 41, and 52) or a southbridge controller (claims 32, 42, or 53), is the source of the SMI. Likewise, because one having ordinary skill in the art at the time the application was filed would have known that a front side bus connects the processor and chipset (*See e.g.,* page 5 of Intel® 810E Chipset: Great Performance for All PCs, Revision 1.3, January 2001; attached herein), applicant's specification supports receiving a message via a front side bus (claims 29, 39, and 50). Accordingly, applicant respectfully requests that the Examiner reconsider and withdraw the rejection of claims 29, 31-32, 39, 41-42, 50, and 52-53 under 35 U.S.C. § 112, first paragraph.

C. Rejections Under 35 U.S.C. § 112, second paragraph

The Examiner rejected claims 1-17 and 26-45 under 35 U.S.C. § 112, second paragraph because it is unclear to the Examiner whether the limitation "an SMI" derives antecedent basis from the preambles of independent claims 1 and 5. As amended, claims 1 and 5 now derive proper antecedent basis from their respective preambles. Accordingly, applicant respectfully requests that this rejection be withdrawn with regard to claims 1 and 5. In addition, applicant respectfully request that the rejection of dependent claims 2-4, 6-17, and 26-45 be withdrawn as well.

D. Rejections Under 35 U.S.C. § 102(e) and 35 U.S.C. § 103(a)

The following discussion provides an overview of the applied references and applicant's technology followed by an analysis of the §§ 102(e) and 103(a) rejections.

1. Applicant's Technology

All of the pending claims are directed to specific manners of executing code when a processor enters SMM. Independent claims 1 and 5 recite "executing code during a SMI" and independent claim 18 recites "instructions for a SMI routine that allows execution of a Portable Executable program."

2. Wooten

The technique described by Wooten changes the architecture of the processor to include a new mode: virtual system mode ("VSM"). (Col. 3, lines 11-13: "the present invention includes a processor having the prior three user addressing modes and a new virtual system mode (VSM)." emphasis added). Wooten's VSM is not system management mode ("SMM").

Indeed, not only does Wooten champion VSM as a new mode, but Wooten also illustrates several disadvantages of SMM as compared to VSM. For example, Wooten describes emulation as a "costly" problem in processors having a SMM. (Col. 10, lines 25-33). Wooten explains that "[i]n a 386 compatible processor, addressing mechanisms cannot be mixed," which "complicates device emulation when using SMM because the SMM code must devote significant amounts of time in an address translation process." (Col. 2, lines 49-67). In contrast to SMM, Wooten boasts that VSM "provides emulation transparently to the operating system and application software...but use[s] very few processor cycles to enter and exit the emulation operations and [does] not hav[e] large address translation burdens." (Col. 3, lines 3-8; Col. 10, lines 43-46).

Also, Wooten provides that "virtual system mode selection is controlled by a bit in the VSM Enable Register 238...and is independent of the user mode." (Col. 7, lines 20-23; emphasis added). In fact, Wooten makes clear that, rather than causing the processor to enter into any new user mode, entry into VSM retains the user mode that was in use prior to entering VSM. (Col. 3, lines 20-23, 35-38; Col. 10, lines 34-37, 43-45). That is, if the processor is in real mode when VSM is entered, it retains real mode; if the processor is in protected mode when VSM is entered, protected mode is retained; and if the processor is in virtual 8086 mode when VSM is entered, virtual 8086 mode is retained.

In VSM, two memory addressing modes are active at the same time: (1) the VSM addressing mechanism and (2) the addressing mechanism of the mode of operation prior to entering VSM (i.e., real mode, protected mode, or virtual 8086 mode). (Col. 3, lines 19-23; Col. 21, lines 14-15; Col. 17, lines 35-39: VSM provides "two addressing modes [that are] active at one time, the short stack as compared to SMM and the detailed information provided, [so that] the emulation can be rapid and efficient." emphasis added). Wooten describes using the segment override bit to distinguish between the VSM address space and the address space of the mode of operation prior to entering VSM. (Col. 3, lines 19-23; 38-41). For example, if while in VSM a segment override is applied, the VSM addressing mechanism will interpret the address using the addressing mechanism of the mode of operation prior to entering VSM (Col. 11, line 1 – Col. 13, line 47). Finally, to exit VSM Wooten describes only three instructions: IRET, RECC, and RENCC. (Col. 3, lines 24-27; Col. 18, lines 28-32).

3. Russell

Russell is directed to a method of managing time between multiple protected mode execution environments. (Col. 2, lines 40-45). To switch between modes, Russell describes a "context register" to indicate which execution environment is active. (Col. 8, lines 55-62). "[O]ne advantage of [Russell's] technique is that it...eliminat[es] the need for an emulator." (Col. 2, lines 55-65).

4. Rejection Under 35 U.S.C. § 102(e)

The Examiner rejected claims 18-25, 46, and 54-55 under 35 U.S.C. § 102(e) over Wooten.

As amended, claim 18 recites "instructions for an SMI routine [performed in response to receipt of the SMI] that allows execution of a Portable Executable program that resides in physical address space above address 0x100000...[and execution of] the Portable Executable program that resides in physical address space above address 0x100000 [before returning from the SMI]."

First, in rejecting independent claim 18, the Examiner argues that in Wooten "code is certainly executed above 0x100000 in a 4GB address space." (Office Action, Page 4). As is discussed above, if while in VSM a segment override is applied, the VSM addressing mechanism will interpret the address using the addressing mechanism of the mode of operation prior to entering VSM (Col. 11, line 1 – Col. 13, line 47). Wooten makes clear that, if while in VSM a segment override is present on an instruction of a program, the segment override will cause the VSM addressing mechanism to erroneously access data in the address space of the mode of operation prior to entering VSM, causing the program to fail. Because Portable Executable programs must have the ability to specify segment override bytes on an instruction to access a code segments (e.g., APIs) or data segment variables, it would be impossible to run a Portable Executable in VSM as described by Wooten. Accordingly, for at least this reason, Wooten fails to teach or suggest the claimed approached of "executing the Portable Executable program that resides in physical address space above address 0x100000 [before returning from the SMI]" as recited by independent claim 18. Therefore, applicant respectfully requests that the Examiner reconsider and withdraw this rejection with regard to claim 18.

Second, the Examiner argues that "claim 18 does not recite any limitations which connect the switch to protected mode to any other limitations in the claim." (Office Action,

Page 15). Although applicant persists in his position that the SMI routine, as originally recited in claim 18, is executed in response to an SMI, applicant herein amends claim 18 to further clarify this point: as amended, claim 18 recites "instructions for an SMI routine...by a method performed in response to receipt of the SMI comprising...switching the processor to protected mode..." That is, switching the processor to protected mode is recited as being part of an SMI routine performed in response to the receipt of an SMI, and thus is performed in SMM.

In contrast to the claimed invention, Wooten fails to teach or suggest switching the processor to protected mode as part of entering VSM. Specifically, entry into VSM is independent of the user mode." (Col. 7, lines 20-23; emphasis added). In fact, Wooten makes clear that, rather than causing the processor to enter into any new user mode, entry into VSM retains the user mode that was in use prior to entering VSM. (Col. 3, lines 20-23, 35-38; Col. 10, lines 34-37, 43-45). In other words, entry into VSM has no effect on the user mode that is selected and does not involve switching the processor to protected mode. To the extent that Wooten can be said to describe entering a different mode upon entering VSM, this mode is VSM itself, not a different user mode such as protected mode. Accordingly, claim 18 is also patentable over Wooten for this reason.

Third, the Examiner asserts that VSM is SMM. (Office Action, Page 6). As was made clear in applicant's October 20, 2005 and July 3, 2006 responses, applicant respectfully disagrees with the Examiner's position that VSM is the same as SMM. Wooten's technique changes the architecture of the processor to include a new mode (Col. 3, lines 11-13: "the present invention includes a processor having the prior three user addressing modes and a new virtual system mode (VSM)." emphasis added). Wooten also describes several disadvantages of SMM as compared to VSM. For example, Wooten explains that "[i]n a 386 compatible processor, addressing mechanisms cannot be mixed" and that this "complicates device emulation when using SMM because the SMM code must devote significant amounts of time in an address translation process." (Col. 2, lines 49-67). Moreover, Wooten trumpets that, as compared to SMM, VSM "provides

emulation transparently to the operating system and application software...but use[s] very few processor cycles to enter and exit the emulation operations and [does] not hav[e] large address translation burdens." (Col. 3, lines 3-8; Col. 10, lines 43-46). Thus, according to Wooten, VSM is clearly not SMM. Therefore, for this reason as well, claim 18 is patentable over Wooten.

Finally, with regard to dependent claim 55, the Examiner asserts that VSM returns by "any means for returning from the SMI." (Office Action, Page 6). However, Wooten fails to teach or suggest "returning from the interrupt by executing an RSM instruction" as recited by claim 55. In fact, exiting in such as manner is incompatible with VSM because Wooten describes only three instructions to exit VSM: IRET, RECC, and RENCC. (Col. 3, lines 24-27; Col. 18, lines 28-32). Clearly, Wooten does not describe exiting VSM by executing an RSM instruction. Therefore, applicant respectfully requests that the Examiner reconsider and withdraw this rejection of claim 55.

For at least the reasons discussed above, applicant respectfully requests that the Examiner reconsider and withdraw the rejection of claim 18 under 35 U.S.C. § 102(e) over Wooten. In addition, because claims 19-25, 46 and 54-55 depend from claim 18, they are allowable for at least the same reasons discussed above.

5. Rejections Under 35 U.S.C. § 103(a)

a. The references, as combined, fail to teach or suggest all the limitations of the claimed invention

The Examiner rejected claims 1-17, 33-34, 43 and 44 under 35 U.S.C. §103(a) over a combination of Wooten and Russell.

The Examiner correctly notes that Wooten fails to teach or suggest "replacing first contents of the global descriptor register that point to a first global descriptor table in use when the system management mode interrupt occurred with a second contents that point

to a second global descriptor table that is distinct from the first global descriptor table" as recited by independent claims 1 and 5. However, the Examiner mistakenly relies upon Russell to disclose this claimed feature. Applicant respectfully disagrees with the Examiner's position.

Russell is directed to a method of managing time between multiple protected mode execution environments. (Col. 2, lines 40-45). To switch between modes, Russell describes a "context register" to indicate which execution environment is active. (Col. 8, lines 55-62). The Examiner argues that the context register of Russell is a global descriptor table register. (Office Action, Page 8). A global descriptor table register holds the base address of a global descriptor table (*See e.g.,* page 11-6 of the Pentium Processor User's Manual, Volume 3: Architecture and Programming Manual), whereas Russell's context register simply indicates which execution environment is active. (Col. 6, lines 39-43; Col. 7, lines 22-25). Moreover, even though Russell discloses that each execution environment contains a global descriptor table register, Russell fails to teach or suggest the claimed approach of "replacing first contents of the global descriptor register that point to a first global descriptor table in use when the system management mode interrupt occurred with a second contents that point to a second global descriptor table that is distinct from the first global descriptor table" as recited by independent claims 1 and 5. For at least this reason, it is clear that Wooten and Russell, individually and in combination, fail to teach or suggest the claimed invention.

In addition, with regard to dependent claims 34 and 44, the Examiner asserts that VSM returns by any means for returning from the SMI. (Office Action, Pages 12 and 6). However, Wooten fails to teach or suggest "returning from the interrupt by executing an RSM instruction" as recited by claims 34 and 44. In fact, exiting in such a manner is incompatible with VSM because Wooten describes only three instructions to exit VSM: IRET, RECC, and RENCC. (Col. 3, lines 24-27; Col. 18, lines 28-32). Because Wooten does not describe exiting VSM by executing an RSM instruction as recited by claims 34

and 44, applicant respectfully requests that the Examiner reconsider and withdraw the rejection with regard to claims 34 and 44.

b. The references, as combined, teach away from the claimed invention

"A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention." (MPEP § 2141.02(VI); emphasis in original). Consequently, a proper rejection cannot simply pick and choose particular elements from Wooten and Russell to find independent claims 1 and 5 unpatentable. It is improper to modify Wooten to arrive at the claimed invention because Wooten teaches away from the claimed invention. Specifically, Wooten teaches away from the claimed invention because Wooten defines a new mode of the processor—VSM—which is not SMM.

Indeed, not only does Wooten define VSM as a new mode, but Wooten also recommends against using SMM. For example, Wooten explains that "[i]n a 386 compatible processor, addressing mechanisms of a processor cannot be mixed between different modes of operation," which "complicates device emulation when using SMM because the SMM code must devote significant amounts of time in an address translation process." (Col. 2, lines 49-67). In fact, Wooten further explains that an "addressing mode change in SMM further exacerbates the overhead problems so that the use of the SMI is not readily feasible." (Col. 2, line 67 – Col. 3, line 2; emphasis added). Because VSM is clearly not SMM, and entering SMM is required by applicant's claims, Wooten teaches away from the claimed invention and it is improper to modify Wooten to render applicant's claims obvious.

c. The references, as combined, teach away from their combination

It is improper to combine Wooten and Russell because the references, as combined, teach away from their combination. (MPEP § 2145(X)(D)(2)). Russell describes a method for switching between execution environments. (Col. 2, lines 40-45).

In contrast, Wooten trumpets a single mode with two memory addressing modes that are active at the same time (Col. 3, lines 19-23, 38-41; Col. 17, lines 35-39). Moreover, Wooten discredits switching between execution environments, in the context of SMM, because of the overhead associated with entering and exiting SMM. (Col. 2, line 63 – Col. 2, line 3: "the full state of the processor [is] saved on entry to SMM and the full state of the processor [is] restored on exit from SMM. These operations require 100's of processor cycles."). In other words, Russell switches between execution environments and Wooten does not. Instead of switching modes, Wooten varies the addressing mechanism on an instruction-by-instruction basis. (Col. 3, lines 19-23; 38-41: "If in VSM and a segment override is applied, the segment override is interpreted according to the addressing mechanism of the mode of operation prior to entering VSM"). Thus, it is improper to combine Wooten and Russell because they teach away from their combination.

Assuming, *arguendo*, that the references can be combined, the potential combination is not sufficient to establish a *prima facie* case of obviousness. "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." (MPEP § 2143.01(III); emphasis in original). This requirement, which demands that there be some teaching, suggestion, or motivation to combine the references, protects against the use of impermissible hindsight reasoning. "Defining the problem in terms of its solution reveals improper hindsight in the selection of the prior art relevant to obviousness." In re Kahn, Fed. Cir. 2006 (quoting Ecolochem, Inc. v. S. Cal. Edison Co., 227 F.3d 1361, 1372 (Fed. Cir. 2000) (quoting Monarch Knitting Mach. Corp. v. Sulzer Morat GmbH, 139 F.3d 877, 881 (Fed. Cir. 1998))). Accordingly, the motivation to combine prior art references must be based upon specific teaching in the prior art, such as a specific suggestion in the prior art reference.

> To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference

> teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.
>
> The *teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art*, not in applicant's disclosure.

In re Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). MPEP § 2143 (emphasis added).

The required motivation to combine Wooten and Russell is not present. The Office Action indicates that one skilled in the art would have been motivated to combine Wooten and Russell "to efficiently run two execution environments." (Office Action, Page 8). To support this assertion, the Examiner relies on Russell, Col. 2, lines 55-65, which provides that "one advantage of [Russell's] technique is that it...eliminat[es] the need for an emulator." However, Wooten describes VSM as "provid[ing] emulation transparently to the operating system and application software...but using very few processor cycles to enter and exit the emulation operations and not having large address translation burdens." (Col. 3, lines 3-8). Because the motivation provided by the Examiner does not support combining the references, applicant respectfully requests that the Examiner reconsider and withdraw this rejection.

d. The combination of Wooten, Russell, and common knowledge in the art does not render the claimed invention obvious

The Examiner rejected claims 47-53 and 56 under 35 U.S.C. §103(a) over a combination of Wooten and common knowledge in the art. In addition, the Examiner rejected claims 26-32, 35-42 and 45 under 35 U.S.C. §103(a) over a combination of Wooten, Russell, and common knowledge in the art.

Claims 26, 27, 29-32, 36, 37, 39-42, 47, 48, and 50-53 are directed to the particular means by which the recited SMM is entered, including: receiving a signal on an input line

of the processor (claims 26, 36, and 47), such as an SMI input line (claims 27, 37, and 48); receiving a message via a front side bus of the processor (claims 29, 39, and 50); in response to a processor chip set (claims 30, 40, and 51), such as a Northbridge controller (claims 31, 41, and 52) or Southbridge controller (claims 32, 42, and 53); and in response to an electronic circuit (claims 33, 43, and 54).

"It is not appropriate for the Examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known." (MPEP § 2144.03; emphasis original). The combinations of Wooten, Russell, and common knowledge in the art do not render claims 26-27, 29-32, 36-37, 39-42, 47 and 50-53 obvious because, while one skilled in the art would know to enter SMM using the recited mechanisms, one skilled in the art would also know that it would be impossible to enter VSM using the recited mechanisms.

Wooten does not teach or suggest entering VSM in any of these recited manners. To the contrary, Wooten describes that "transitions from the user modes to VSM can be made by indirect calls through a call gate, such as by a jump or call instruction, or through vectored entries, such as a hardware interrupt or I/O fault." (Col. 3, lines 24-27) Because Wooten fails to teach or suggest entering the recited system management mode in any of the manners recited by these claims, applicant respectfully requests that the Examiner reconsider and withdraw this rejection. If the Examiner maintains this rejection, applicant requests that the Examiner provide documentary evidence supporting the assertion that it was common knowledge at the time of the invention to enter VSM using the recited mechanisms.

Therefore, for at least the reasons stated above, the suggested combination does not render applicant's claims obvious, and applicant respectfully requests that the rejection of claims 1 and 5 be withdrawn. In addition, because 2-4, 6-17, 26-27, 29-34, 36-37, and 39-44, 47 and 50-53 depend from claims 1 and 5, they are allowable for at least the same reasons.

E. Conclusion

For the reasons discussed above, applicant submits that all of the pending claims are in condition for allowance. If the Examiner has any questions or believes a telephone conference would expedite prosecution of this application, the Examiner is encouraged to call the undersigned at (206) 359-8077.

Applicant believes all fees due in connection with this response are submitted herewith. However, if a fee is due, please charge our Deposit Account No. 50-0665, under Order No. 149148001US1 from which the undersigned is authorized to draw.

Dated: 7/16/07

Respectfully submitted,

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